

PART OF CPS FC200

TELETYPEWRITER CONTROLLER INTERFACE
AND TIMING CIRCUITS

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CHANNEL INTERFACE CIRCUITS
ELEMENT IDENTIFICATION

TERM. MOD.	FNCT.	TERM.	LOC.
010N	I	303	2A1
010P	I	203	2A0
011N	I	002	2A2
011P	I	101	2A1
EN0B0	I	207	2A2
EN0B0	I	307	2A2
10P11	I	306	2A2
10P10	I	103	2A5
10P10	I	208	2A1
10P10	I	302	2A2
10P10	I	102	2A4
080N	#	305	2G1
080P	#	206	2G2
081N	#	304	2G2
081P	#	205	2G2
100	#	201	2G0
10P11	#	003	2G5
10P0	#	202	2G0
10N	#	108	2G3
10P	#	005	2G3
11N	#	104	2G4
11P	#	004	2G4
1A0T0	#	301	2G1
SHFT0	#	308	2G0
ZACT0	#	300	2G0

SYMBOL

LINE INTERFACE CIRCUITS
ELEMENT IDENTIFICATION

TERM. MOD.	FNCT.	TERM.	LOC.
AL00	I	017	3A3
AL00	I	116	3A4
ALCO	I	015	3A5
ALDO	I	014	3A5
R00	I	016	3A3
R00	I	115	3A4
R00	I	114	3A5
R00	I	113	3A4
TP00	I	210	3A6
TP00	I	213	3A7
TP00	I	109	3A0
TP00	I	110	3A0
FR01	#	214	3G3
FR01	#	215	3G4
FR01	#	216	3G5
FR01	#	217	3G6
SALM01	#	009	3G3
SALM01	#	011	3G4
SALM01	#	115	3G5
SALM01	#	316	3G5
S00	#	310	3G6
S00	#	309	3G7
S00	#	108	3G8
S00	#	008	3G9
+3	P	000	3G0
+24	P	013, 112	3G1
+24	P	019, 118	3G2
+24	P	218, 318	3G1
GR0	C	200, 319	3G1
GR0	C	000	3G1

LINE TIMING CIRCUITS
ELEMENT IDENTIFICATION

TERM. MOD.	FNCT.	TERM.	LOC.
LT1N01	#	204	2G7

RECORD OF CHANGES

DWG. ISS.	PREV. FURN.	STD.	MFR. DISC.	SEE NOTE

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	FC200
CONNECTOR ON FRAME	972A OR 972C
ACCEPTABLE SERIES	7

NOTES:

- GROUND RETURN.
- UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS.
CAPACITANCE VALUES ARE IN MICROFARADS.
VALUES PRECEDED BY THE SYMBOL + (PLUS)
OR - (MINUS) ARE IN VOLTS.
- BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS.

IC CODE	BAT. TERM.	GRD. TERM.
155A	14	1
41N	3, 6, 7, 8	1, 2
41NE	14	2, 8
41DL	14	8

- BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
-24	218, 318
+3	000
+24	019, 118
+24F	013, 112
GR0	200, 319, 000

- HORIZONTAL MOUNTING CENTERS AT 0.5 INCH.

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	1H

CURRENT DRAIN.

+2V	300mA
+24V	150mA
-24V	50mA

NOTICE - NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

3A

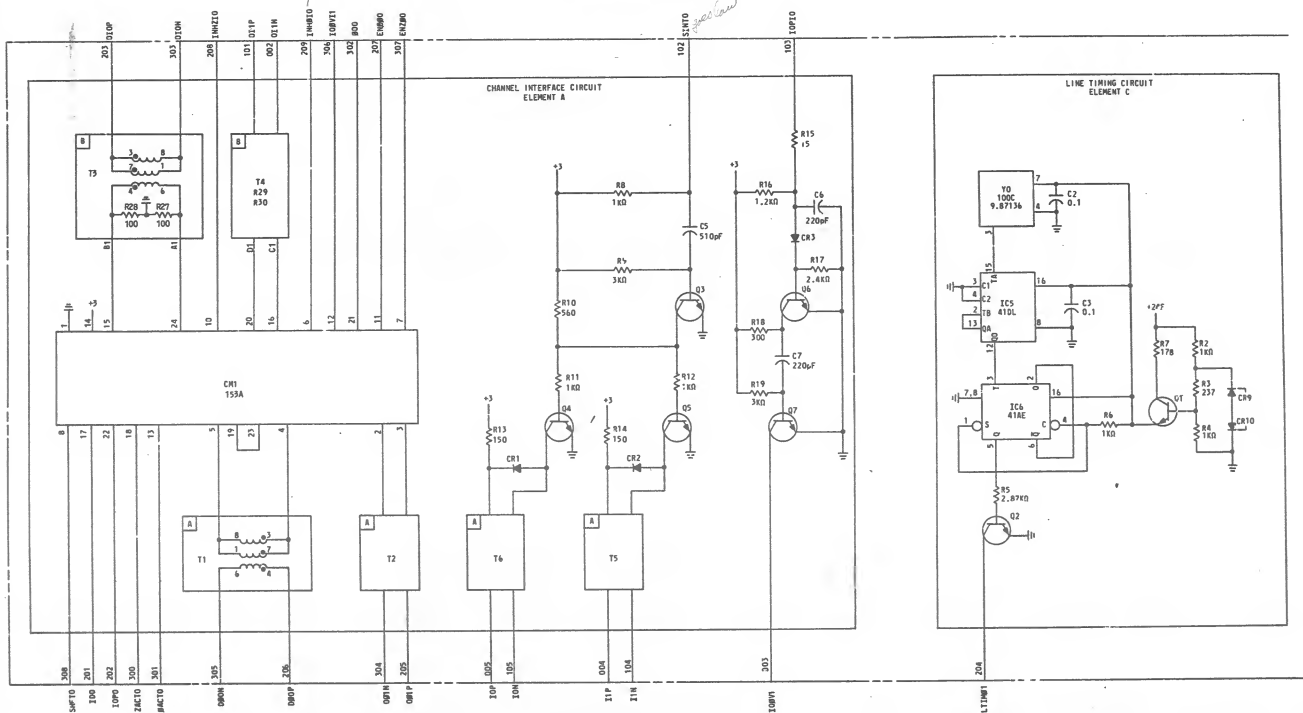
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FC200 CIRCUIT PACK

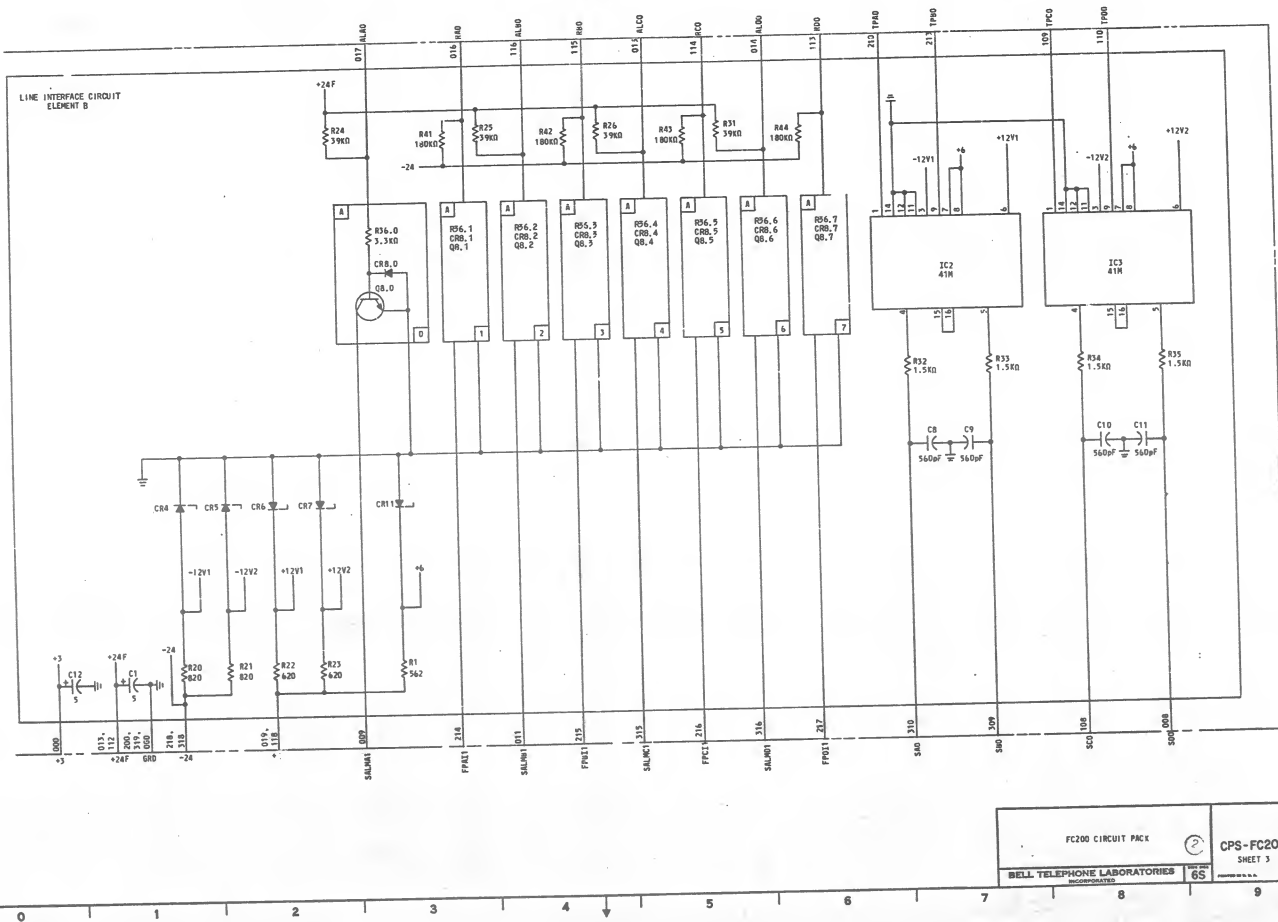
TELETYPEWRITER CONTROLLER
INTERFACE AND TIMING
CIRCUITSBELL TELEPHONE LABORATORIES
INCORPORATEDAT&T
STANDARDCPS-FC200
7 SHEETS

65

PART OF CPS FC200 TELETYPEWRITER CONTROLLER INTERFACE AND TIMING CIRCUITS



PART OF CPS-FC200 TELETYPEWRITER CONTROLLER INTERFACE AND TIMING CIRCUITS



CPS-FC200

TELETYPEWRITER CONTROLLER INTERFACE AND
TIMING CIRCUITSTELETYPEWRITER CONTROLLER INTERFACE AND
TIMING CIRCUITS

RESISTOR (CONT)

DESIG

DESIG	CODE	
R17	KS-1664S L1	2.4KΩ
R18	KS-1664S L1	300
R19	KS-1668S L1	3KΩ
R20	KS-19150 L1	820
R21	KS-19150 L1	820
R22	KS-19150 L1	62C
R23	KS-19150 L1	620
R24	KS-1664S L1	39KΩ
R25	KS-1664S L1	39KΩ
R26	KS-1664S L1	39KΩ
R27	KS-1664S L1	100
R28		

R32

R32	KS-16645	L1,	1.5KΩ
R33	KS-16645	L1,	1.5KΩ
R34	KS-16645	L1,	1.5KΩ
R35	KS-16645	L1,	1.5KΩ
R36, C-R36, 2	KS-16645	L1,	1.5KΩ

R43
R48

R43	KS-1664S	L1, 180KΩ
R44	KS-1664S	L1, 180KΩ

TRANSFORMER

TRANSFORMER	
DESIG	CODE
T1	2664G
T2	
T3	
T4	
T5	
T6	2664G

TRANSISTOR

TRANSISTOR	CODE
Q1	92A
Q2	66S
Q3	
Q4	
Q5	
Q6	
Q7	
Q8.0-Q8.7	66S

A. FUNCTION

A. FUNCTION
CIRCUIT PACK (CP) FC200 IS USED IN THE TELETYPEWRITER CONTROLLER (TTYC) CIRCUIT TO INTERFACE THE TTYC LOGIC CIRCUITRY TO THE 3A CENTRAL CONTROL [3A CC] AND THE TELETYPEWRITER [TTY].

LEADS HAVING DESIGNATION THAT END IN D ARE LOW WHEN ACTIVE OR IN THE ONE STATE. LEADS HAVING DESIGNATION THAT END IN 1 ARE HIGH WHEN ACTIVE OR IN THE ONE STATE.

CHANNEL INTERFACE CIRCUIT - ELEMENT A

DATA IS PASSED BETWEEN THE 3A CC TO THE TTYS IN SERIAL BINARY CIRCUIT FROM A CONTINUOUS LINE OF DATA. THE 3A CC'S IS TERMINATED BY TRANSMISSIONS T3 AND TA AND THEIR ASSOCIATED RECEIVERS. CIRCUIT MODULE (CH 1) CONVERTS THE BIPOLAR INPUT DATA TO LOGIC-LEVEL SIGNALS. DATA ON LEAD IN0, A TIMING SIGNAL, IS ALSO GENERATED BY CIRCUIT MODULE (CH 1) AND IS SHIFTED TO THE TTYC CIRCUITS VIA SAMPLE LEAD IN0 WHEN IT IS STABLE. (REFER TO THE DESCRIPTION CDS 1534 FO) THE RELATIONSHIP BETWEEN THE BIPOLAR INPUT AND LOGIC LEVEL TIMING SIGNALS IS AS FOLLOWS: LEAD IN0 IS HIGH WHEN LEAD IN0 IS HIGH AND LEAD IN0 IS LOW WHEN LEAD IN0 IS LOW. LEAD IN0 IS ACTIVE WHEN LEAD IN0 IS ACTIVE WHEN DATA IS BEING RECEIVED FROM CCR OR CCT. THESE LEADS ARE CONNECTED TO THE OPPOSITE CC INPUT CONTROL LEAD (LEAD IN0) OF THE OTHER CHANNEL. WHEN LEAD IN0 IS HIGH, LEAD IN0 IS LOCK OUT ONE CC WHILE AN INPUT IS BEING RECEIVED FROM THE OTHER.

TDPO IS ACTIVE WHILE INPUT DATA IS PRESENT. IT CAN BE CONNECTED TO TDPID WHERE IT WILL TURN OFF Q6 AND ALLOW C7 TO CHARGE TO +5 VOLTS THROUGH R16. WHEN THE INPUT DATA STOPS, TDPO IS NO LONGER ACTIVE AND C6 CHARGES TO +3V THROUGH R16. WHEN IT REACHES APPROXIMATELY 1.5 VOLTS, C6 WILL TURN ON Q6 AND DISCHARGE C7. Q7 WILL CUT OFF UNTIL C7 CAN CHANGE ITS CHARGE THROUGH R19 TO ABOUT 0.7 VOLTS IN THE OPPOSITE DIRECTION. THIS RESULTS IN A NOMINAL 450ns PULSE ON LEAD TDPIV. TDPIV IS CONNECTED TO TDPIVI WHERE IT INITIALIZES CIRCUITS IN CM1. THIS SIGNAL CAN ALSO INITIALIZE OTHER TTY LOGIC CIRCUITS.

DATA IS SENT FROM THE TTTC TO THE 3A CC'S IN BIPOLAR FORM VIA COAXIAL CABLE CONNECTED TO D00P/N AND D01P/N. THE LOGIC - LEVEL SIGNAL OF DATA 'G' BE OUTPUTTED IS SET ON LEAD 000. TIMING FOR THE OUTPUT DATA IS DERIVED FROM AN ALL - ZERO'S INPUT DATA STREAM THAT IS SUPPLIED BY THE 3A CC DURING THE TIME WHEN THE TTTC IS EXPECTED TO OUTPUT DATA TO IT. LEADS EN20 AND ENB00 ENABLE THE OUTPUT DATA TO BE DIRECTED TO 3A C00 OR 3A C01.

LEAD SINTO IS ACTIVATED BY THE TTYC WHEN IT HAS COMPLETED A CHARACTER EXCHANGE WITH THE TTY. WHEN SINTO IS NOT ACTIVE, CS IS CHARGED TO ABOUT 10 VOLTS THROUGH R8. WHEN SINTO GOES ACTIVE, CS IS DISCHARGED AND CS VOLTS UNTIL C7 CAN CHANGE ITS CHARGE THROUGH R9. THIS RESULTS IN A NOISE BURST OUT OF C7. A 103 HZ SIGNAL IS SENT TO BOTH 3A CC'S IN DRIVERS Q4 AND Q5 AND TRANSFORMERS T5 AND T6. THIS SIGNAL IS CONNECTED TO THE 3A CC INTERRUPT CIRCUITS WHEN THE 3A CC IS USED IN A SYSTEM THAT SERVICES ITS TTY'S ON A DEMAND BASIS.

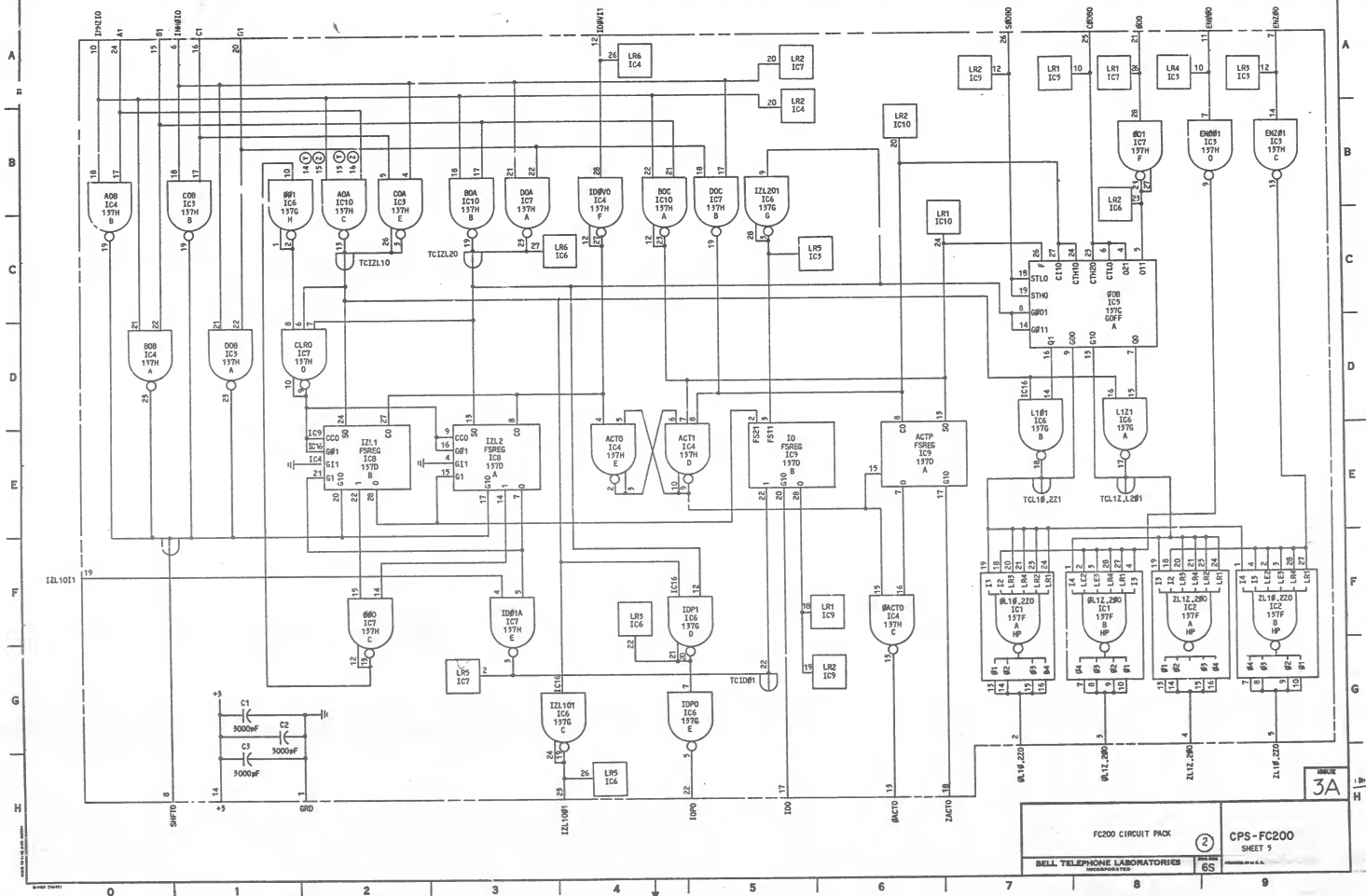
TO IS A CRYSTAL CONTROLLED OSCILLATOR WITH A FREQUENCY OF 9.87136MHZ. IC5 IS A 4-STAGE RIPLEE COMUTER. IC6 IS A TOGGLE F/F. IC5 AND IC6 OVIDE THE OSCILLATOR OUTPUT BY 52 TO PRODUCE A 30B.48KHZ TUSC (3.21TUSC PERIOD) OUTPUT AT TERMINAL 204. Q2 INTERFACES THIS SIGNAL TO THE TTYC LOGIC WHERE IT IS USED TO DETERMINE BIT TIMING FOR THE CHARACTER EXCHANGED WITH THE TTY. Q1 IS A 5 VOLT REGULATOR TO SUPPLY TO, IC5 AND IC6.

[illegible]

C. SYMBOL/LEAD MIMICRY

MEMORIAL

[illegible]



PART OF CMS 153A

COMPONENT LIST INTEGRATED CIRCUIT

LOC CODE FLEM ID	IC1 157F (NOTE 1) DESIG SH LOC	IC2 157F (NOTE 1) DESIG SH LOC	IC3 157H DESIG SH LOC	IC4 157H DESIG SH LOC	IC5 157C DESIG SH LOC	IC6 157B DESIG SH LOC	IC7 157H DESIG SH LOC	IC8 157D DESIG SH LOC	IC9 157D DESIG SH LOC	IC10 157H DESIG SH LOC	LOC CODE ELEM ID
A	RL1F.220 SF7	2L12.200 SF8	D08 501	B08 530	908 568	L121 518	D04 583	I2L2 513	ACT9 514	B0C 584	A
B	RL1F.200 SF8	2L10.220 SF9	C08 501	A08 580		L101 507	D0C 585	I2L1 512	ID 515	B0A 583	B
C			EN201 589	RACTD 596		I2L101 544	B0D 592			A0A 582	C
D			EN001 509	ACT1 514		I201 594	CL0D 501				D
E			C04 582	ACT0 514		I200 565	I201A 593				E
F			RACTD 593	I200V 584			901 588				F
G						I2L201 585					G
H						901 581					H

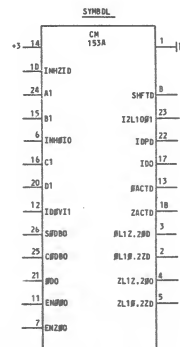
CAPACITOR

DESIG	CODE
[3] C1-C3	B01A 3000pF

NOTES:

1. CAPACITOR CHIP B01A, 3000pF IS BONDED ON EACH SIDE OF 157F SIC.

RECORD OF CHANGES				
DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE
3	2	Y	2	



BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

IC CODE	BAT TERM	GRD TERM
157C	25	11
157D	25	11
157F	25, 26	11, 12
157G	25	11
157H	25	11

SUPPORTING INFORMATION

CATEGORY	NO
INTEGRATED CIRCUIT CODE	153A
ACCEPTABLE SERIES	3-4,4

FC200 CIRCUIT PACK

BELL TELEPHONE LABORATORIES

153A IC

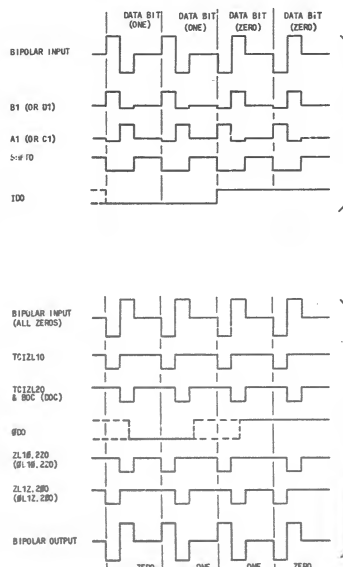
CPS-FC200
SHEET 6

6S

3A

00523-8-840

TIMING DIAGRAM

FIG. 1
BIPOLAR TO LOGIC
LEVEL CONVERSION
USING CN 193AFIG. 2
LOGIC LEVEL TO
BIPOLAR CONVERSION
USING CN 193A

CIRCUIT DESCRIPTION

A. FUNCTION

CN 193A IS USED IN THE CONVERSION BETWEEN BIPOLAR SIGNALS ON THE 3A CC 1/2 DATA LINES AND LOGIC-LEVEL SIGNALS REQUIRED BY PERIPHERAL UNIT CONTROLLER CIRCUITS (SUCH AS THE TTY CONTROLLER).

B. DETAILED DESCRIPTION

LEADS HAVING DESIGNATIONS THAT END IN 1 ARE HIGH WHEN ACTIVE, OR IN THE ONE STATE. LEADS HAVING DESIGNATIONS THAT END IN 0 ARE LOW WHEN ACTIVE, OR IN THE ONE STATE. FLIP-FLOPS ARE SET TO THE ONE STATE AND CLEARED TO THE ZERO STATE.

BIPOLAR TO LOGIC LEVEL CONVERSION

THE CONTROLLER RECEIVED DATA LINE IS TRANSFORMER-COUPLED TO CN 193A ON LEADS A1 AND D1 FROM CCO, AND C1 AND D1 FROM CCI. THE DATA IS SORTED BY GATES A0A AND D0A AT TC12L10, AND BY GATES B0A AND D0A AT TC12L20. THE RELATIONSHIP BETWEEN THE BIPOLAR DATA, THE INPUT TO CN 193A, AND ITS LOGIC-LEVEL DATA (LEAD) AND TIMING (SHIFT) OUTPUT SIGNALS, IS SHOWN IN FIG. 1. THE LOGIC POSITIVE AND NEGATIVE EXCURSIONS, A LOGICAL ONE IS A POSITIVE LOGIC FOLLOWED BY A NEGATIVE LOGIC. A LOGICAL ZERO IS A NEGATIVE LOGIC FOLLOWED BY A POSITIVE LOGIC. CLIPPING CIRCUITS, WHICH ARE PART OF GATES TO WHICH THE A1, B1, C1, AND D1 INPUTS CONNECT, LIMIT THE NEGATIVE EXCURSION AT THIS POINT, AND PREVENT RECOVERY PROBLEMS IN THESE GATES.

THE INPUT DATA LEAD (100) IS SET AT THE LEADING EDGE OF THE FIRST LOSE. THE TIMING SIGNAL IS THE TRAILING EDGE OF S-SHIFT WHICH OCCURS AT THE TRAILING EDGE OF THE SECOND LOSE. THUS, THE CONTROLLER IS SIGNALLED TO SAMPLE THE INCOMING DATA IN THE CENTER OF THE BIT PERIOD WHEN THE DATA LEAD IS STABLE. CARE HAS BEEN TAKEN TO MINIMIZE THE NUMBER OF GATES THAT CONTROL THE 100 AND SHFT LEADS IN ORDER THAT VARIATIONS IN GATE DELAYS WILL NOT DESTROY THE RELATIONSHIP BETWEEN THESE SIGNALS. NOMINAL TIMES FOR THE 3A CC SERIAL 1/2 DATA ARE A 10-MS-BIT INTERVAL WITH 97.5-MS LOSES.

THE SHFT LEAD IS CONTROLLED BY GATES A0B, B0B, C0B, AND D0B, AND FLIP-FLOPS 12L1 AND 12L2. INITIALLY, NONE OF THE GATES ARE ACTIVE AND BOTH FLIP-FLOPS ARE IN THE CLEARED STATE SO THAT SHFT IS HIGH. IF B0B AND D0B ARE NOT ACTIVE, THE FIRST LOSE OF THE INPUT DATA WILL ACTIVATE ONE OF GATES (DEPENDS ON WHETHER THE BIT IS A ONE OR ZERO AND IF IT IS FROM CCO OR CCI) AND PULL SHFT LOW. THE FIRST LOSE WILL ALSO ACTIVATE ONE OF THE GATES FORMING TC12L20 OF TC12L20 WHICH WILL SET ONE OF THE FLIP-FLOPS, 12L1 OR 12L2, DEPENDS ON CONDITIONS PREVIOUSLY DESCRIBED. THE PURPOSE OF THESE FLIP-FLOPS IS TO HOLD SHFT LOW DURING ANY GAP THAT MIGHT BE PRESENT BETWEEN THE FIRST AND SECOND LOSES AND TO PREVENT THE SECOND LOSE FROM CHANGING THE STATE OF THE DATA FLIP-FLOP (10).

WHEN THE SECOND LOSE OF THE INCOMING DATA BIT IS ACTIVE THE WATE OF THE GATE ACTIVATED BY THE FIRST LOSE WILL BE ACTIVE AND IT WILL ALSO HOLD SHFT LOW (A0B AND B0B ARE WATES AS ARE C0B AND D0B). THIS LOGIC WILL ALSO SET THE FLIP-FLOP (12L1 OR 12L2) THAT WAS NOT SET BY THE FIRST LOSE. WHEN THE SECOND FLIP-FLOP IS SET, IT INHIBITS THE PATH BY WHICH THE FIRST FLIP-FLOP WOULD SHFT TO GROUND. WHEN THE FIRST LOSE IS OVER ONLY THE GATE ACTIVATED BY THE SECOND LOSE HOLDS SHFT LOW.

WITH BOTH FLIP-FLOPS SET, THE INPUT TO C10D FROM B01 IS HIGH. THE OTHER INPUTS TO C10D, 100 AND TC12L10 ARE CONTROLLED BY THE DATA LOSES. WHEN THE FIRST LOSE IS GONE, ONLY THE SECOND LOSE CONTROLS C10D. WHEN THE SECOND LOSE EXPIRES, THE GATE HOLDING SHFT IS DEASELED AND SHFT WILL GO HIGH. C10D WILL GO LOW AT THIS TIME AND CLEAR BOTH FLIP-FLOPS. C10D LOW ALSO DUCKS THE 12L1 AND 12L2 CONNECTION TO SHFT SO THAT FALSE SIGNALS CANNOT OCCUR ON THIS LEAD AS THE FLIP-FLOPS CHANGE FROM THE 11 TO THE 00 STATE.

LEAD 100 IS CONTROLLED BY THE TO FLIP-FLOP. IT RETAINS THE LAST INCOMING DATA STATE UNTIL IT IS UPDATED BY THE FIRST LOSE OF A NEW DATA BIT. IF THE NEW DATA BIT IS A ZERO, TC12L10 WILL BE ACTIVE FIRST AND DRIVE GATE 12L10 HIGH. TERMINALS 19 AND 23 ARE EXTERNALLY TIED TOGETHER SO THAT 12L10 HAS BOTH INPUTS HIGH. IT SHOULD BE NOTED THAT 12L1 AND 12L2 ARE INITIATED FROM THE CLEARED STATE AND THAT TC12L10 SETS 12L1 BUT DOES NOT AFFECT 12L2. 12L1A WILL PULL 12L1 LOW, WHICH WILL CLEAR 10 AND DRIVE 100 HIGH, TO ITS ZERO STATE. WHEN THE SECOND LOSE IS ACTIVE FOR THE ZERO DATA BIT, TC12L20 WILL DRIVE 12L2 HIGH. HOWEVER, 12L2 WILL BE SET BY THE FIRST LOSE, IN ORDER TO PREVENT 12L201 FROM CHANGING THE 10 FLIP-FLOP.

IF THE INCOMING DATA BIT IS A ONE, TC12L20 WILL BE ACTIVE FIRST. 12L201 WILL BE HIGH UNTIL 12L1 IS CLEARED, AND THE TO FLIP-FLOP, 12L1, WILL BE SET. 100 WILL THEN BE LOW, WHICH IS THE ONE STATE. WHEN THE SECOND LOSE IS ACTIVE FOR AN INCOMING ONE, TC12L10 IS ACTIVE, AND WILL DRIVE 12L10 HIGH. TC12L20, HOWEVER, WILL HAVE SET 12L2, WHICH PREVENTS 12L1A FROM CHANGING 10.

LEADS ZACTO AND BACTO INDICATE WHICH, IF ANY, CC IS ACTIVELY COMMUNICATING WITH THE CONTROLLER. THE ACT FLIP-FLOP, FORMED BY GATES ACTO AND ACT1, IS SET BY GATES BOC OR DOO TO INDICATE THAT ONE OF THE CC'S IS SUPPLYING INPUT DATA. FLIP-FLOP ACTP IS SET BY DOO WHEN CC1 IS ACTIVE, AND IS CLEARED BY DOO WHEN CC2 IS ACTIVE. THE ACT AND ACTP FLIP-FLOPS ARE COMBINED TO ACTIVE ZACTO WHEN CC1 IS ACTIVE AND BACTO WHEN CC1 IS ACTIVE. BOTH THE ZACTO AND BACTO ARE HIGH WHEN NEITHER CC IS ACTIVE.

INWZD AND INWZD BLOCK INPUT DATA FROM CCO AND CCI WHEN THEY ARE ACTIVE.

LEAD 10P0 WILL BE ACTIVE WHEN EITHER LOSE OF THE INPUT DATA BIT IS PRESENT. IT CAN BE USED BY AN EXTERNAL CIRCUIT TO INDICATE WHEN INCOMING DATA IS PRESENT. THE EXTERNAL CIRCUIT MUST HAVE SUFFICIENT FILTERING TO HOLD OVER ANY GAP BETWEEN LOSES.

INPUT B0P1 IS USED TO INITIALIZE THE 12L1 AND 12L2 TO THE 00 STATE, AND TO CLEAR THE ACT FLIP-FLOP. THIS SIGNAL MAY BE ACTIVATED BY AN EXTERNAL CIRCUIT AT THE END OF A DATA COMMUNICATION.

LOGIC LEVEL TO BIPOLAR CONVERSION

THE 3A CC FOLLOWS THE DATA PORTION OF A COMMUNICATION TO A PERIPHERAL UNIT WITHIN AN ALL-ZEROS INPUT BIT STREAM. THIS BIT STREAM IS USED BY THE PERIPHERAL UNIT AS BIT TIMING FOR THE BIPOLAR DATA SET TO THE 3A CC. THE 3A CC WAITING FOR THE ZEROS BIT STREAM UNTIL IT RECEIVES A REPLY FROM THE PERIPHERAL UNIT, OR UNTIL THE WAITING INTERVAL, IN WHICH IT MUST RECEIVE A REPLY IS EXCEEDED. THUS, FOR EACH OUTGOING BIT PERIOD, LEAD A1 (OR C1) IS ACTIVE FOLLOWED BY B1 (OR D1) ACTIVE. INPUTS ENO0 AND ENO00 ARE ACTIVATED TO START THE OUTPUT AND DIRECT IT TO CCO OR CCI.

GATES ZL16, Z20 AND ZL12, Z80 ARE TRANSFORMER-COUPLED TO THE OUTGOING DATA LINE TO CCO. GATES #L10, Z20 AND #L12, Z80 ARE TRANSFORMER-COUPLED TO THE OUTGOING DATA LINE TO CCI. THESE GATES ARE HELD HIGH DURING THERE IS NO INCOMING DATA OR WHEN THE ENABLE LEAD (EN000, EN000) IS NOT ACTIVE.

THE RELATIONSHIP BETWEEN THE ALL-ZEROS INPUT DATA, THE LOGIC LEVEL OUTGOING DATA LEAD, AND THE BIPOLAR OUTPUT DATA IS SHOWN IN FIG. 2. THE LOGIC LEVEL OUTGOING DATA SIGNAL (DOO) IS TROGLED INTO PHO0R TO THE BIT PERIOD. THE OUTPUT OF DOO IS COMBINED WITH THE TIMING SIGNALS DERIVED FROM THE INCOMING DATA (TC12L10 AND TC12L20) TO DETERMINE THE ORDER IN WHICH ZL16, Z20 AND ZL12, Z80 WILL BE ACTIVE. IF A ONE IS TO BE SENT, TC12L16, Z21 WILL BE ACTIVE DURING THE FIRST LOSE AND TC12L12, Z81 WILL BE ACTIVE DURING THE SECOND LOSE. THE REVERSE WILL BE TRUE TO OUTPUT A ZERO. THESE SIGNALS WILL BE INVERTED BY THE ENABLED OUTPUT GATES ZL10, Z20 AND ZL12, Z80 AND/OR #L10, Z20 AND #L12, Z80.

A GATE IN EACH PAIR IS CONNECTED TO THE OPPOSITE END OF THE PRIMARY OF A TRANSFORMER. EACH PAIR OF GATES IS PROVIDED WITH A TRANSFORMER. THUS, THE ORDER IN WHICH THE GATES ARE ACTIVE DETERMINES THE POLARITY OF THE PULSE AVAILABLE AT THE TRANSFORMER SECONDARY.

NOTE THAT THE INVERTING INPUTS TO THE INVERTING INPUTS (OR BOC OR DOO) DURING THE BIT INTERVAL PRECEDING THAT IN WHICH THE BIT IS TROGLED INTO THE INPUTS SH00D AND PH00D ARE DIRECT SET AND CLEAR OPERATIONS ON B0B.

SYMBOL LEAD

C. MECHANICS

JUNCTIONS

ACTP

ACTO

A1B1

BOC0

C1D1

EN000

EN00

EN000

10P0

12L1

12L2

12L1A

12L2A

B0B

B0C0

B0C0

B0C0

B0C0

B0C0

B0C0

B0C0

B0C0

B0C0

B0C0

B0C0

B0C0

B0C0

DEFINITION

SET OR CLEARED TO DETERMINE WHICH INPUT PORT IS ACTIVE

SET BY GATES ACTO AND ACT1. INPUT PORT IS ACTIVE

INPUTS FROM CCI

CLEAR BOC

ENABLE OUTPUT TO CCI

ENABLE OUTPUT TO CCO

INCOMING DATA

INCOMING DATA PRESENT

INCOMING DATA ZERO TIME - SET BY FIRST LOSE WHEN INPUT IS ZERO

INCOMING DATA ZERO TIME - SET BY SECOND LOSE WHEN INPUT IS ZERO

INCOMING DATA

CC1 IS ACTIVE

OUTGOING DATA BIT

OUTGOING DATA

FIRST LOSE FOR A ONE, SECOND LOSE FOR A ZERO TO CCI

FIRST LOSE FOR A ONE, SECOND LOSE FOR A ONE TO CCI

SHFT

SET OR FF

ZACTO

ZL16, Z20

ZL12, Z80

FIRST LOSE FOR A ONE, SECOND LOSE FOR A ONE TO CCO

FIRST LOSE FOR A ONE, SECOND LOSE FOR A ONE TO CCO

F2000 CIRCUIT PACK

BELL TELEPHONE LABORATORIES

SERIAL NO. 153A

CPS-FC200

SHEET 7

24